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09/905,318	07/13/2001	William C. Altmann	19570-05858	6174

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EXAMINER	
NATNAEL, PAULOS M	

ART UNIT	PAPER NUMBER
2614	9

DATE MAILED: 07/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/905,318	ALTMANN, WILLIAM C.	
	Examiner	Art Unit	
	Paulos M. Natnael	2614	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-16 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-16 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. The Claims **4,5,10,11,15,16** are objected to because of the following informalities: TMDS and LVDS should be defined. Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims **1-16** are rejected under 35 U.S.C. 103(a) as being unpatentable over **MacInnis** et al., U.S. Pat No. **6,738,072** in view of **Admitted Prior Art (APA)**.

Considering claim **1**, **MacInnis et al** discloses the following claimed subject matter, note;

a) a digital video scaler (DVS) for scaling the digital video received from..., is met by video scaler 52, Fig.5;

b) a constant frequency clock connected to the DVS, is implied because without a clock or timing signal the scaler 52 may not be synchronized properly. See also the disclosure on col. 11, lines 23-27 where MacInnis et al. disclose that the video compositor preferably provides final output signal to the **data size converter 190, which serializes the 16-bit word sample into an 8-bit word sample at twice the clock frequency**, and provides the 8-bit word sample to the video encoder 62).

c) a multiplexer for selecting either the scaled digital video from the DVS and the digital video from the host system of the current stage, is met by Mux 188, fig.5, which selects the scaled image output from scaler 52 or the un-scaled image output from video FIFO 148.

Except for;

d) the preceding stage to a constant resolution;

Regarding c), **MacInnis** et al discloses a graphics display system with anti-flutter filtering and vertical scaling feature. The system of **MacInnis** et al is utilized in a set-top box. Although a preceding stage and/or a next stage are not specified in the **MacInnis** et al reference, it would be obvious to those with ordinary skilled in the art that the preceding stage would be the video source or head-end and the next stage would be the television set itself. The APA discloses such stages as shown in the Figures 1 and 2. Therefore, it would have been obvious to the skilled in the art at the time the invention was made to modify the system of MacInnis by providing the prior art system in Figures 1 and 2 of the APA in order to better synchronize the transmission of video

signal from one stage (head-end) to the receiver or television set so that flicker or flutter is minimized.

Considering claim **2**, the system of claim 1, wherein said DVS comprises: a retiming FIFO for retiming the received video received from the preceding stage; and a scaling engine for scaling the retimed video data to match the constant resolution, is met by Line Buffer 178 and Scaler Engine 182 Fig.5, respectively.

Considering claim **3**, the system of claim 1, further comprising a receiver for receiving a signal containing digital video from the preceding stage, is met by MPEG Decoder 160, fig.5;

Considering claim **4**, the system of claim 1, wherein said signal is a TMDS signal.

Regarding claim 4, MacInnis et al. discloses CLUT interface and high speed I/O bus system. MacInnis et al and the APA do not disclose a TMDS signal. However, the Examiner takes Official Notice in that Transition Minimized Differential Signaling (TMDS) is notoriously well known in the art, and therefore, it would have been obvious to the skilled in the art to modify the system of MacInnis and the APA as modified above by providing a TMDS capability so that the combined system would be versatile and more useful to the user.

Considering claim **5**, the system of claim 1, wherein said signal is an LVDS signal.

Regarding claim 5, MacInnis et al. discloses CLUT interface and high speed I/O bus system. MacInnis et al and the APA do not disclose a LVDS signal. However, the Examiner takes Official Notice in that Low-voltage differential signaling (LVDS) is notoriously well known in the art, and therefore, it would have been obvious to the skilled in the art to modify the system of MacInnis and the APA as modified above by providing a LVDS capability so that the combined system would be versatile and more useful.to the user.

Considering claim **6**, the system of claim 1, wherein said signal contains audio, is met by audio input 34, fig.1;

Considering claim **7**, a method of transmitting from a current stage having a host system to a next stage with limited clock jitter, a signal containing either digital video from a preceding stage or digital video from the host system of the current stage, comprising the steps of: scaling the digital video received from the preceding stage to a constant resolution using a constant frequency clock; and selecting between the scaled digital video and the digital video from host system of the current stage.

Claim 7 is a method claim of claim 1 and, therefore, claim 7 is rejected for the same reasons as in claim 1.

Considering claim **8**, the method of claim 7, wherein said step of scaling comprises the steps of: retiming the digital video received from the preceding stage; and creating video data matching the constant resolution from the retimed video data.

Claim 8 is a method claim of claim 2 and, therefore, claim 8 is rejected for the same reasons as in claim 2

Considering claim **9**, the method of claim 7, wherein said step of scaling further comprises the step of superimposing an on-screen display (OSD) message, is met by Fig.31 where an embodiment is illustrated which is a flutter filtering and graphics scaling circuit.

Considering claim **10**, the method of claim 7, wherein the signal is a TMDS signal.

Regarding claim 10, see rejection of claim 4.

Considering claim **11**, the method of claim 7, wherein the signal is an LVDS signal.

Regarding claim 11, see rejection of claim 5.

Considering claim **12**, the method of claim 7, wherein the signal contains audio.

Regarding claim 12, see rejection of claim 6.

Considering claim **13**, a method of transmitting from a current stage having a host system to a next stage with limited clock jitter, a signal containing either digital video

from a preceding stage or digital video from the host system of the current stage, comprising the steps of: selecting between the scaled digital video from the preceding stage and the digital video from the current stage; and scaling the selected digital video to a constant resolution using a constant frequency clock.

Regarding claim 13, see rejection of claim 1.

Considering claim **14**, the method of claim 13, wherein said step of scaling the selected digital video comprises the steps of: retiming the selected digital video using a FIFO; and creating video data matching to the constant resolution from the retimed data.

Regarding claim 14, see rejection of claim 2.

Considering claim **15**, the method of claim 13, wherein the signal is a TMDS signal.

Regarding claim 15, see rejection of claim 4.

Considering claim **16**, the method of claim 13, wherein the signal is an LVDS signal.

Regarding claim 16, see rejection of claim 5.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Macaluso et al., U.S. Patent No. **6,380,797** discloses a low voltage differential signal (LVDS) driver circuit.

Kim et al., U.S. Patent No. **6,463,092** discloses a system and method for sending and receiving data signals over a clock signal lines and discloses the Transition minimized differential signal (TMDS) as one of the data communication method utilized in the system..

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paulos M. Natnael whose telephone number is (703) 305-0019. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Miller can be reached on (703) 305-4795. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PMN
July 1, 2004

PAULOS M. NATNAEL
PATENT EXAMINER